REMARKS

The enclosed is responsive to the Examiner's Office Action mailed on March 17, 2008. At the time the Examiner mailed the Office Action claims 1, 2, 4-8, 10-15, 17, and 18 were pending. The Applicants respectfully request reconsideration of the present application and the allowance of all claims now represented.

Claim Rejections

35 U.S.C. 102(e) Rejections

Claims 1, 2, 4-8, 10-15, 17, and 18 stand rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent 5,430,851 (hereinafter "Hirata").

Applicant respectfully submits that Hirata at least does not describe what Applicant's claim 1, 7, or 13 requires. Specifically, Hirata does not describe (underlining added for emphasis not to indicate added/amended words of the claim):

> 1. A processor, comprising:
>
> a plurality of pipelined functional units for executing instructions;
>
> a centralized scheduler, coupled to the plurality of functional units, wherein the centralized scheduler is programmed to receive via an instruction buffer and an instruction decoder at least two separate instruction groups, in a first stage map each of the at least two separate instruction groups to at least a portion of the functional units independently of each other in which the centralized scheduler treats each instruction group as having full access and availability to the plurality of pipelined functional units, and based at least in part on functional unit availability and instruction dependencies, perform a merging and remapping of the at least two separate instruction groups to the at least a portion of the functional units in a second stage to ensure that no resource conflict occurs between the plurality of pipelined functional units.

7. A machine-readable medium having stored thereon a plurality of executable instructions, the plurality of instructions comprising instructions to:

receive at least two separate instruction groups in a scheduler via an instruction buffer and an instruction decoder;

in a first stage of the scheduler, map each of the at least two separate instruction groups to at least a portion of functional units independently of each other; and

based at least in part on functional unit availability and instruction dependencies, perform a merging and remapping of the at least two separate instruction groups to the at least a portion of functional units in a second stage of the scheduler.

13. A method for dispersing instructions to executed by a processor, comprising:

receiving at least two separate instruction groups in a scheduler via an instruction buffer and an instruction decoder;

in a first stage of the scheduler, mapping each of the at least two separate instruction groups to at least a portion of functional units independently of each other; and

based at least in part on functional unit availability and instruction dependencies, performing a merging and remapping of the at least two separate instruction groups to the at least a portion of functional units in a second stage of the scheduler.

The Office Action identifies Hirata's instruction setup units 34 as comprising the first stage and the instruction schedule unit 35 as comprising the second stage. (Office Action mailed March 17, 2008, p. 3)

Applicant, however, submits that Hirata does not teach a centralized scheduler wherein the scheduler is programmed to "in a first stage, map at least two separate instruction groups to at least a portion of the functional units independently of each other in which the centralized scheduler treats each instruction group as having full access and availability to the plurality of pipelined functional units." Hirata describes that "the decode unit **12** *checks*

data dependencies and controls interlocks. . ." and the decode unit is contain within the instruction setup unit **14**. (Hirata Fig. 3; emphasis added). Furthermore, dependency analysis is performed in the dependency analysis unit **13** which is contained within the instruction setup unit **14**. (Hirata Fig. 3; emphasis added) "The dependency analysis unit **13** memorizes and manages *which register the instruction in execution phase is inputted or outputted from*." (Hirata Col. 6, ll. 8-10) Applicant respectfully submits, therefore, that the first stage does not "map at least two separate instruction groups to at least a portion of the functional units *independently* of each other. . ." Even if the instruction setup unit can be construed as performing a first mapping, which the Applicant does not concede that it can be construed as such, this mapping cannot be read as being performed independently of each instruction group.

Applicant respectfully submits that Hirata does not describe "based at least in part on functional unit availability and instruction dependencies, perform a merging and remapping of the at least two separate instruction groups to the at least a portion of the functional units in a second stage to ensure that no resource conflict occurs between a plurality of pipelined functional units." The Office Action points to the instruction setup unit as the second stage. (Office Action mailed March 17, 2008 p. 3) Applicant points out that the instruction schedule unit does not perform a merging or remapping of instructions. "The instruction schedule unit **15** inputs an instruction type tag T and operational directive information C from the decode unit **12** and outputs a receiving state signal D." (Hirata Col. 6, ll. 19-22) Even if setting the type tag T can be considered a first mapping of the instruction to an execution unit, and Applicant does not concede that it can be, the instruction schedule unit **15** does not perform a merging or remapping. At no point does the instruction schedule unit **15** remap an instruction a function execution unit, but rather the instruction schedule unit **15** utilizes previous mappings as the unit "inputs *an instruction type tag T*. . . The instruction type tag T indicating to which function execution unit the operational directive information C inputted from the decode unit **12** is sent. . ." (Hirata Col. 6, ll. 19-27) The instruction schedule unit **15** merely uses

type tag T to identify which execution unit receives which instructions, and this is not a remapping of an instruction. Thus, Hirata does not describe "merging and remapping of the at least two separate instruction groups to the at least a portion of the functional units" in a second stage.

The Office Action points to column eight lines forty-eight to fifty-six as describing a second stage that remaps based on function unit availability. (Office Action mailed March 17, 2008, p. 3). However, further down in that paragraph, Hirata describes that "the units **16-18** report to the *dependency analysis units* **13** that the dependency among the instructions have been eliminated." (Hirata Col. 8, ll. 57-59; emphasis added) Therefore, the dependency analysis units take into account instruction dependencies as does the decode units **12**, as discussed above. These units, being part of the instruction setup unit **14**, are utilized in the first stage in Hirata, not in the second stage.

Applicant respectfully submits, therefore, that Hirata does not describe what is required by independent claims 1, 7, and 13. Claims 2 and 4-6 are dependent upon claim 1 and allowable for at least the same rational. Claims 8 and 10-12 are dependent upon claim 7 and are allowable for at least the same rational. Claims 14-15 and 17-18 are dependent upon claim 13 and are allowable for at least the same rational. In light of the comments above, the Applicants respectfully request the allowance of all claims.

CONCLUSION

Applicant respectfully submits that all rejections have been overcome and that all pending claims are in condition for allowance.

If there are any additional charges, please charge them to our Deposit Account Number 02-2666. If a telephone conference would facilitate the prosecution of this application, the Examiner is invited to contact David F. Nicholson at (408) 720-8300.

Respectfully submitted,

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